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10/730,321	12/08/2003	Toshiaki Fukushima	JP920030131US2	2430

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EXAMINER
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VIDWAN, JASJIT S

ART UNIT	PAPER NUMBER
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2182

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06/25/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/730,321	<b>Applicant(s)</b> FUKUSHIMA ET AL.	
	<b>Examiner</b> JASJIT S. VIDWAN	<b>Art Unit</b> 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 December 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 21 and 24-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21, 24, 28-34, 36-39 is/are rejected.
- 7) ☒ Claim(s) 25-27, 35 and 40 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Allowable Subject Matter*

1. Claims 25, 26, 27, 35, 40 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

1. Applicant's arguments filed 12/10/07 have been fully considered but they are not persuasive.

Applicant argues:

- a. Claim 31 – As amended, prior art fails to teach first memory attribute information and the acquired second memory attribute information to include Serial Presence Detect Information.
  - b. Claim 21 & 36 – Prior art fails to teach determining the transfer rate setting value based at least in part upon the upper limit temperature.
2. With respect to argument a, **Examiner disagrees**. First of all, Applicant claims that Thomann and Pollard combined do not teach the above limitation. However, as was indicated in office action mailed on 09/18/2007, combination of above stated references with that of Jeddelloh taught said limitation of attribute information including serial presence detect information [**see Jeddelloh, Paragraph 0005**]. Even excluding Jeddelloh reference, Pollard teaches the said limitation wherein the ROM is a serial presence detect device storing design characteristics [**see Pollard, Col. 3, Lines 33-39**].
3. With respect to argument b, **Examiner disagrees**. The cited Pollard section (Col. 3, Lines 30-48) teach memory module therein storing memory characteristics of said module including, number of devices on the module, power consumption, heat spreader design data, a maximum allowable junction temperature..." Based in part to the above characteristics in addition to thermal environment characteristics of the system the memory modules are operating in, the BIOS determines the "maximum sustainable power level." Pollard goes further to disclose that once the maximum sustainable power level is determined, the BIOS further translate this power level into maximum performance characteristics [**see Pollard, Col. 4, Lines 30-36**].

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 31, 32, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann et al U.S. Pub No: 2002/0169922 [**herein after Thomann**] and Pollard, II et al U.S. Patent No: 7,050,959 [**herein after Pollard**].

2. **As per Claim 31**, Thomann teaches a method for setting a data transfer rate [**Paragraph 0010, "...read/write timing calibration of these memory devices..."**] for multiple memory modules [**see Fig. 1, element 30, "memory modules"** – Though Fig. 1 is labeled as "prior art," Thomann teaches that his system may be used with any conventional memory architecture or computer system such as element 5 in figures 1-4 (all labeled "Prior art")] comprising processor [**see Fig. 1, element 10**] that is configured to execute the instructions in memory:

- (a) Receiving memory module attribute information [**see Paragraph 0056, "Characteristics of each memory device"**] from each memory module in the multiple memory module [**Paragraph 0056, "In either instance, the characteristics of each memory device 100 in the computer system 5 must be known in order to select an appropriate data clock delay for each DQ line for each memory device 100 for each memory module 30 or for the system (i.e. all memory modules 30) as a whole"**]
- (b) Individually determining data transfer rates [**"Data clock delay" – see Paragraph 0054 – "Selection of the data clock delay is critical for high frequency applications, such as in the 300MHz to 500 MHz range, in order to provide optimum data transfer rates and to insure reliable data transfer."**] for each memory module in the multiple memory modules based at least in part upon the corresponding received memory module

attribute information [see Thomann, Paragraph 0063, “For DQ level calibration, read/write timing calibration is performed individually for all DQ lines on all memory modules 30 within the system”]

(c) Collectively setting a data transfer rate with respect to the multiple memory modules based at least in part on the individually determined data transfer rates [see Thomann, Paragraph 0063, “For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line”]

Thomann teaches the above limitations, however fails to explicitly state that memory module attribute information (“characteristics of each memory device”) is received from attribute memories in each memory. Pollard of analogous art of setting data transfer rates based on certain characteristics of individual memory module teaches the above limitation of storing the attribute information in the memory of each module [See Pollard, Col. 5, Lines 30-37 - - Also see Fig. 2, elements 202 & 204]. Furthermore, Pollard teaches a system wherein the acquired memory attribute information includes Serial Presence Detect information [see Pollard, Col. 3, Lines 33-39].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Thomann with that of Pollard in order to take advantage of individually calculating the optimum power performance for each memory module based on its individual physical limitations (characteristics) rather than simply pre-selecting a “lowest” processing power whereby wasting valuable bandwidth and/or processing power [see Col. 1, Lines 23-38]. Therefore, it is for the above stated reason that one of ordinary skill would have been motivated to combine the teachings of Thomann with that of Pollard in order to maximize the physical limitations of every individual memory module within a system [Col. 1, Lines 23-38].

3. **As per Claim 38**, Thomann as modified by Pollard above teaches a computer-readable medium comprising computer-executable instructions for:

(a) Acquiring memory attribute information [see Thomann, Paragraph 0056, “Characteristics of each memory device”] for each memory module in a plurality of

memory modules [see Thomann, Paragraph 0056, “In either instance, the characteristics of each memory device 100 in the computer system 5 must be known in order to select an appropriate data clock delay for each DQ line for each memory device 100 for each memory module 30 or for the system (i.e. all memory modules 30) as a whole”], wherein each of the memory modules include an attribute memory that retains the memory attribute information [See Pollard, Col. 5, Lines 30-37 -  
- Also see Fig. 2, elements 202 & 204]

(b) Accessing a setting value candidate database [see Pollard, Col. 4, Lines 27-29, “Lookup table”]

(c) Locating candidate data transfer rate setting values from each memory module in the plurality of memory modules in the setting value candidate database, wherein the candidate data transfer rate setting values correspond to the acquired memory attribute information in the setting value candidate database [see Pollard, Col. 4, Lines 15-27 –  
The influence coefficients stored in BIOS 110 have major impact on determining the maximum sustainable power based on the acquired characteristics of the system including airflow rates, specific module layout and integrated circuit packaging - - System is similar to that of Thomann wherein the characteristics include operating voltage and operating temperature among other things (see Thomann, Paragraph 0055)].

(d) Determining a data transfer rate setting value that is to be applied with respect to each memory module in the plurality of memory modules based at least in part upon the located candidate data transfer rate setting values [see Thomann, Paragraph 0063, “For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line”]

(e) Outputting the selected data transfer rate setting [“single data clock delay”] value to a host controller that controls data transfer with respect to the plurality of memory

modules [see Thomann, Paragraph 0026, “The memory devices also receive one or more clock signals over the memory bus, the clock signals being provided by the processor, memory controller or another component of the computer system as desired”]

4. **As per Claim 32**, Thomann and Pollard as modified by Huang teaches a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises:

(a) Determining a maximum data transfer rate with respect to data transfer rates determined for each memory module [see Pollard, Col. 4, Lines 46-57]

(b) Determining a minimum data transfer rate with respect to data transfer rates determined for each memory module [see Pollard, Col. 3, Lines 40-52]

(c) Collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate [see Pollard, Col. 5, Lines 4-9]

5. **As per Claim 36**, Thomann as modified by Pollard teaches an apparatus wherein the memory comprises additional instructions for:

(a) Acquiring a first and second upper limit temperature at which the first and second memory module is operated externally through a host controller [see Pollard, Col. 3, Lines 30-40, “Maximum allowable junction temperature”]

(b) Determining the first and second data transfer rate setting value based at least in part upon the first and second upper limit temperature [see Pollard, Col. 3, Lines 40-48]

3. Claims 21, 22, 24, 29, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann et al U.S. Pub No: 2002/0169922 [herein after Thomann] and Pollard, II et al U.S. Patent No: 7,050,959 [herein after Pollard] further in view of Huang, U.S. Pub No: 2003/0095464 [herein after Huang]

6. **As per Claim 21**, Thomann teaches a method for setting a data transfer rate [**Paragraph 0010**, **“...read/write timing calibration of these memory devices...”**] for multiple memory modules [**see Fig. 1, element 30, “memory modules”** – Though Fig. 1 is labeled as “prior art,” Thomann teaches that his system may be used with any conventional memory architecture or computer system such as element 5 in figures 1-4 (all labeled “Prior art”)] comprising:

- (a) Receiving memory module attribute information [**see Paragraph 0056**, **“Characteristics of each memory device”**] from each memory module in the multiple memory module [**Paragraph 0056**, **“In either instance, the characteristics of each memory device 100 in the computer system 5 must be known in order to select an appropriate data clock delay for each DQ line for each memory device 100 for each memory module 30 or for the system (i.e. all memory modules 30) as a whole”**]
- (b) Individually determining data transfer rates [**“Data clock delay”** – **see Paragraph 0054** – **“Selection of the data clock delay is critical for high frequency applications, such as in the 300MHz to 500 MHz range, in order to provide optimum data transfer rates and to insure reliable data transfer.”**] for each memory module in the multiple memory modules based at least in part upon the corresponding received memory module attribute information [**see Thomann, Paragraph 0063**, **“For DQ level calibration, read/write timing calibration is performed individually for all DQ lines on all memory modules 30 within the system”**]
- (c) Collectively setting a data transfer rate with respect to the multiple memory modules based at least in part on the individually determined data transfer rates [**see Thomann, Paragraph 0063**, **“For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line”**]

Thomann teaches the above limitations, however fails to explicitly state that memory module attribute information (“characteristics of each memory device”) is received from attribute memories in each memory. Pollard of analogous art of setting data transfer rates based on certain characteristics of



individual memory module teaches the above limitation of storing the attribute information in the memory of each module **[See Pollard, Col. 5, Lines 30-37 - - Also see Fig. 2, elements 202 & 204]**. Pollard further teaches using an upper limit temperature at which each memory module in the multiple memory module is operated in order to determine the data transfer rate **[Col. 3, Lines 30-48 – further see Col. 4, Lines 30-32]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of Thomann with that of Pollard in order to take advantage of individually calculating the optimum power performance for each memory module based on its individual physical limitations (characteristics) rather than simply pre-selecting a "lowest" processing power whereby wasting valuable bandwidth and/or processing power **[see Col. 1, Lines 23-38]**. Therefore, it is for the above stated reason that one of ordinary skill would have been motivated to combine the teachings of Thomann with that of Pollard in order to maximize the physical limitations of every individual memory module within a system **[Col. 1, Lines 23-38]**.

Thomann and Pollard above fail to teach a system wherein memory module attribute information includes position wherein the memory slot the said memory modules are located and based on this information to determine what transfer rate to apply. Huang of analogous art teaches the above limitation of determining which memory location the memory modules is located and applying transfer cycle rate to the said memory modules accordingly **[see Huang, Paragraph 0026]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to take advantage of providing different rates according to the distance between the control chipset and each memory unit so that memory access may attain an optimum efficiency **[see Huang, Paragraph 0022]**.

7. **As per Claim 22**, Thomann and Pollard as modified by Huang above teaches a method further comprising receiving an upper limit temperature at which each memory module in the multiple memory modules is operated **[see Thomann, Paragraph 055, "operating temperature" / also see Pollard Col.**

**3, Lines 30-39, “maximum allowable junction temperature”]**, wherein the data transfer rates are individually determined for each memory module in the multiple memory modules based at least in part upon the received upper limit temperature **[see Thomann, Paragraph 0063, “For DQ level calibration, read/write timing calibration is performed individually for all DQ lines on all memory modules 30 within the system”]**

8. **As per Claim 34**, see rejection of Claim 21

9. **As per Claim 24**, Thomann and Pollard as modified by Huang above teaches a method wherein the data transfer rate set collectively for the multiple memory modules is an upper limit value of a data transfer rate **[see Pollard, Col. 4, Lines 46-57]** at which a host controller accesses one of the multiple memory modules relative to a maximum data transfer rate at which the host controller can access the one of the multiple memory modules **[see Thomann, Paragraph 0063, “For device level calibration, a single data clock delay is selected to provide reliable data transfer on all DQ lines of a given memory device such that data transmission on any DQ line”]**

10. **As per Claim 29**, Thomann and Pollard as modified by Huang teaches a method wherein setting a data transfer rate with respect to the multiple memory modules collectively comprises transferring the data transfer rate with respect to the multiple memory modules to a host controller **[see Thomann, Paragraph 0026, “The memory devices also receive one or more clock signals over the memory bus, the clock signals being provided by the processor, memory controller or another component of the computer system as desired”]**

11. Claims 28, 33 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann and Pollard and further in view of Mylly, U.S. Pub No: 2005/0235110 **[herein after Mylly]**.

12. **As per Claim 28, 33 and 39**, Thomann and Pollard teach the limitations of Claims 21, 31 and 38, however fail to teach a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises determining a minimum data transfer rate with respect to data transfer rates determined for each memory module and using the minimum data transfer rate as the collective data transfer rate for the multiple memory modules. Mylly, in an analogous art of setting data

transfer rate of memory modules, teaches the above missing limitation of a method wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises determining a minimum data transfer rate with respect to data transfer rates determined for each memory module [see **Mylly, Page 7, Paragraph 0105, “communication property information of low values – lowest performance limits of connected memory modules”**] and using the minimum data transfer rate as the collective data transfer rate for the multiple memory modules [Page 4, Paragraph 0059, “...data transfer bus may be operated by a default setting of the communication properties in order to allow the communication with all connected memory modules (default setting comprise low clock frequency)”].

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings above in order to take advantage of making sure that at a minimum, all connected memory modules are able to operate and no single memory module is handicapped by a unsustainable clock frequency [see **Paragraph 0055**]. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the teachings above to take advantage of making sure that at a minimum, all connected memory modules are able to operate and no single memory module is handicapped by a unsustainable clock frequency [see **Paragraph 0055**].

13. Claims 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomann and Pollard and further in view of Jeddelloh, U.S. Pub No: 2002/0144173 [**herein after Jeddelloh**].

14. **As per Claim 30**, Thomann as modified by Pollard teach the limitations of Claim 31, however fail to teach a system wherein the attribute information within at least one memory module of the multiple memory modules includes manufacturer identification information that indicates a manufacturer of the at least one memory module. Jeddelloh teaches the above limitation in disclosing a method wherein the attribute information within at least one memory module of the multiple memory modules includes manufacturer identification information that indicates a manufacturer of the at least one memory module [see **Jeddelloh, Page 3, Claim 6**] number of devices information that indicates a number of devices on the at least one memory module [see **Jeddelloh, Page 3, Claim 4, “...the number of components in each said memory module”**], memory bank information that indicates whether the at least one memory

module is of a single-sided or of a double sided implementation [see Thomann, Paragraph 0023, “Single in-line memory module (“SIMM”) or dual in-line memory module (“DIMM”)”] and type identification information that identifies a type of the at least one memory module [see Jeddeloh, Paragraph 0032, “type of memory module”]

15.

It would have been obvious to one of ordinary skill in the art at the time of Applicant’s invention to combine the above teachings in order to take advantage of having a memory controller that selects the speed of the memory address/data bus and memory clock based on data identifying memory components which are stored in serial presence detect EEPROM [see Jeddeloh, Paragraph 0006]. It is for this reason that one of ordinary skill in the art at the time of Applicant’s invention would have been motivated to combine the above teachings in order to take advantage of having a memory controller that selects the speed of the memory address/data bus and memory clock based on data identifying memory components which are stored in serial presence detect EEPROM [see Jeddeloh, Paragraph 0006].

### ***Conclusion***

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASJIT S. VIDWAN whose telephone number is (571)272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV  
2/26/08

/Tariq Hafiz/  
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